Innovative Time-Domain Smart Temperature Sensor Design

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Introduction

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- **Majors**
  - Analog IC design & layout
  - Time-domain signal processing circuits
  - Patent infringement
Guidelines

- Introduction
- Voltage-Domain Smart Temperature Sensor
- Time-Domain Smart Temperature Sensor
- Fully Digital Smart Temperature Sensor
- Conclusion
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What is temperature?

- Operational definition
  - A measure of the average translational **kinetic energy** associated with the disordered microscopic motion of atoms and molecules.

\[
\left[ \frac{1}{2}mv^2 \right]_{\text{average}} = \frac{3}{2} kT
\]

If the temperature of two objects is the same, then their average translational KE is the same. Their internal energies and specific heats will not necessarily be the same.

镚 Temperature demo

[Wikipedia]
Thermal Couple

Voltage \propto\ Temperature
Thermistor

Integrated passive SAW-IDT temperature sensor

From: Meijer et al, 1994

From: Bao et al, 1994
Applications

TPMS: embedded pressure, temperature, acceleration sensors for tires with RF Tx/Rx

Domestic animal monitoring
Digital Thermometer
Structural Health Monitoring System

- ensure the structural integrity by monitoring the response of the building.
- measure strain, displacement and temperature.

![Structural Health Monitoring System Diagram](image-url)
Body Sensor Network
Guidelines

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Voltage-Domain Predecessors

- Parasitic BJT used
- Subtle calibration circuits adopted
  - chopping and dynamic element matching (DEM)
  - second-order curvature correction
  - offset cancellation
  - $\Delta \Sigma$ modulator
- High accuracy OPAMP with large number of input bits

Smart Temperature Sensor

Temperature Sensor

Bandgap Reference

A/D Converter

Digital Output
Some History

- **CMOS smart temperature sensor with 120mW power consumption in 1990** [A. Bakker, JSSC 1996]
  - temperature sensor made of lateral bipolar transistors, fabricated in special process
  - some *curvature* on characteristic curve
  - To be more compatible with standard CMOS technologies, vertical substrate BJT used instead

- **Subtle and time-consuming calibration process at two temperatures by an external microcontroller adopted**
  - measurement *error* reduced from $\pm 7^\circ C$ to $\pm 1^\circ C$
  - die area was 1.5mm$^2$ in a 0.7-um CMOS process
Calibration done at the wafer probe by poly fuse trimming [M. Tuthill, JSSC 1998]

- error reduced from +1°C ~+5°C to ±1°C with external reference
- die area increased to 3.3mm² in a 0.6-µm process

un-calibrated accuracy of 1°C at room temperature achieved by utilizing chopper and dynamic element matching (DEM) techniques

2nd-order curvature correction combined with chopper and DEM techniques ensures a 3σ accuracy of 1.5°C under batch calibration [M. Pertijs, ISCAS 2001]
±0.5°C (3σ) accuracy achieved by combining offset cancellation, DEM, and curvature correction techniques with calibration at room temperature after packaging [M. Pertijs, ISSCC 2003]

Another improved version presented soon to reach an error of ±0.1°C (3σ) → State of the art

- using DEM, chopped current gain independent PTAT bias circuit, and low-offset second-order sigma-delta ADC combined chopping & correlated double sampling
- the spread of the $V_{BE}$ characteristics of substrate PNP transistors needed to be compensated by trimming
- 4.5mm$^2$ chip size in 0.7-μm process and 75μA current consumption [Kofi, ISSCC, JSSC 2005]
Alternatively, frequency-output-based and duty-cycle-output-based temperature sensors

- so-called “quasi-digital” sensors
- chip size extremely small
- simple output digitization with a stable reference clock
- poor accuracy

Most smart sensors focused on error reduction

- more elaborate calibration, larger size & power
- zoom ADC adopted for 7-fold energy saving [Kofi, ISSCC 2010]^1
- using 65nm NPN transistor to get $\pm 0.2^\circ C$ ($3\sigma$) inaccuracy and 0.1mm$^2$ core area [Kofi, ISSCC 2010]^2
State-of-the-Art Chip

- 4.5mm² chip size with 0.7μm 2M-1P process
- -55°C – 125°C Temperature range
- 75μA consumed current
- ±0.1°C Inaccuracy ($3\sigma$)
- 16-bit sigma-delta DAC

[M Pertijs, ISSCC 2005]
Industry’s Highest Accuracy Temp Sensors

- ±0.5°C Accuracy over a Wide Temperature Range
- -55°C to +125°C Operating Range
- 2.7V to 5.5V or 1.7V to 3.7V (DS620) Supply Range
- User-Selectable 9- to 12-Bit Resolution
- No External Components Required to Measure Temperature
- Thermostat/Alarm Functionality with User-Defined Nonvolatile Thresholds
# Common Specifications

<table>
<thead>
<tr>
<th></th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Accuracy</td>
<td>0.3</td>
<td>3</td>
<td>°C</td>
</tr>
<tr>
<td>Resolution</td>
<td>0.05</td>
<td>1</td>
<td>°C</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>2.5</td>
<td>5</td>
<td>V</td>
</tr>
<tr>
<td>Supply current</td>
<td>50</td>
<td>500</td>
<td>μA</td>
</tr>
<tr>
<td>Speed</td>
<td>1</td>
<td>50</td>
<td>Samples/s</td>
</tr>
</tbody>
</table>
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- Voltage-Domain Smart Temperature Sensor
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Why Not Voltage-Domain?

- Too many successful predecessors
- Not Innovative
- Hard to digitized
- High cost, high power
  - But very excellent accuracy
Voltage Discrimination

Voltage

Hard limit (V_{CC} or V_{FS})

2^N - 1
2^N - 2

\approx

Sensor output

V_{A}

V_{D}

V_{os}

Voltage-domain

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Process Scaling Down

- Supply Voltage down with process scaling
- Hard limit with resolution and accuracy in voltage-domain.
Why Time-Domain?

- Scalable with process
- Smaller sampling window (dead zone)
- No hard limit for operation range
- Simpler circuit
- Lower chip size and cost
Time-Domain Block Diagram

- Cost reduction
- Low power
- Easy realization
  - TDC instead of ADC used

Input: Temp-to-Time Generator

Process: Time Reference

Output: Digital Output

Time-to-Digital Converter (TDC)
Time-Domain Footprint

- **First chip using delay line for thermal sensing** [P. Chen, JSSC 2005]
  - -0.7°C~+0.9°C inaccuracy from 0°C to 100°C
  - 10µW@2 S/s power and 0.175mm² core size
  - 2-point calibration required

- **Dual-DLL structure with one-point calibration support** [K. Woo, ISSCC 2009]
  - -1.8°C~2.3°C inaccuracy from 0°C to 100°C
  - 0.24µJ per averaged sample, 0.12mm² core size
  - With 3rd master curve for 5 test chips

- **Power consumption lowered as 104nW@25 S/s for RFID tag** [J. Yin, ISSCC 2010]
  - -1.1°C~0.4°C inaccuracy from -20°C to 30°C
First Time-Domain Version

- Temperature-to-time generator
  - Temperature-to-Pulse Generator
- Time-to-digital converter
  - Cyclic TDC
- Time reference
  - Eliminated!
Temperature-to-Pulse Generator

- utilizing gate delays to generate the thermally sensitive pulse
Thermal Characteristic of NOT Gates

- high-to-low and low-to-high propagation time

\[ t_{PHL} = \frac{2 C_L V_{TN}}{k_N (V_{DD} - V_{TN})^2} + \frac{C_L}{k_N (V_{DD} - V_{TN})} \ln \left( \frac{1.5 V_{DD} - 2 V_{TN}}{0.5 V_{DD}} \right) \]

\[ t_{PLH} = \frac{-2 C_L V_{TP}}{k_P (V_{DD} + V_{TP})^2} + \frac{C_L}{k_P (V_{DD} + V_{TP})} \ln \left( \frac{1.5 V_{DD} + 2 V_{TP}}{0.5 V_{DD}} \right) \]

- Where \( k_N = \mu_N C_{ox} (W/L)_N \), \( k_P = \mu_P C_{ox} (W/L)_P \) and \( C_L \) are the transconductance parameters and effective load capacitance.

- Ignore the effects of velocity saturation and other non-idealities & equivalent NMOS and PMOS assumed

\[ T_P = \frac{T_{PLH} + T_{PHL}}{2} = \frac{(L/W) C_L}{\mu C_{OX} (V_{DD} - V_T)} \ln \left( \frac{1.5 V_{DD} - 2 V_T}{0.5 V_{DD}} \right) \]
Both mobility and threshold voltage are thermal sensitive with

$$\mu = \mu_o \left( \frac{T}{T_0} \right)^{km}$$

$km$ in the range of -1.2 to -2.0

$$V_T(T) = V_T(T_0) + \alpha (T - T_0)$$

$\alpha$ depends on the substrate doping level and the implant dose used during fabrication.

$$-0.5 \text{ mV/}^\circ\text{K} < \alpha < -3.0 \text{ mV/}^\circ\text{K}$$

thermal effect of $(V_{DD}-V_T)$ term in denominator somehow be countervailed by $\ln[(1.5V_{DD}-2V_T)/0.5V_{DD}]$ term in numerator

For digital gates, $V_{DD} \gg V_T$, thermal effect dominated by $\mu \rightarrow$ delay↑ as $T↑ \approx \text{PTAT}$
Temperature Characteristic of TDDL

- width of the output pulse at the lower Temperature bound $>> 0$
  - cause large offset
    - long conversion time & more output bits required
  - timing reference delay line (TRDL) added to reduce the measurement offset or adjust the measurement range

![Diagram of temperature characteristic of TDDL](image)
Modified Temperature-to-Pulse Generator

Less offset

START

Temperature Dependent Delay Line

Temperature Reference Delay Line

XOR

$T_p$
Thermal-Compensation Circuit for TRDL

- **Thermal compensation circuit**

  - NOT gate = the same in TDDL
  - P1, P3 and N1 all diode connected → saturation

  \[
  I_{D,P3} = \frac{1}{2} \mu C_{OX} \left( \frac{W}{L} \right) (V_{GS,P3} - V_T)^2 (1 + \lambda V_{GS,P3})
  \]

  By substituting thermal dependence of \( \mu \) & \( V_T \)

  \[
  I_{D,P3} = \frac{1}{2} \mu_0 C_{OX} \left( \frac{W}{L} \right) \left( \frac{T}{T_0} \right)^{km} \left[ V_{GS,P3} - V_T (T_0) - \alpha (T - T_0) \right]^2 (1 + \lambda V_{GS,P3})
  \]

  For \( T > 200^\circ K \), significant plateau effect observed for drawn & effective L
  → channel length modulation term \((1 + \lambda V_{GS,P3})\) will be neglected

  - **For minimum thermal sensitivity, let \( ID,P3/\partial T=0 \)**

  \[
  \frac{u_0 \cdot C_{OX} \cdot km}{2T_0} \left( \frac{W}{L} \right) \left( \frac{T}{T_0} \right)^{km-1} \left[ V_{GS,P3} - V_T (T_0) - \alpha (T - T_0) \right]^2 (1 + \lambda V_{GS,P3})
  \]

  \[
  -\alpha \cdot u_0 \cdot C_{OX} \left( \frac{W}{L} \right) \left( \frac{T}{T_0} \right)^{km} \left[ V_{GS,P3} - V_T (T_0) - \alpha (T - T_0) \right](1 + \lambda V_{GS,P3}) = 0
  \]
After simplification

\[ V_{GS,P3} = V_T(T_0) + \alpha(T - T_0) + \frac{\alpha \cdot T}{km} \]

P1 and N1 sizes adjusted to make \( V_{GS,P3} \) fit the requirement as closely as possible.

substituting \( V_{GS,P3} \) back into current eq.

\[ I_{D,P3} = \frac{1}{2} \mu_0 C_{OX} \left( \frac{W}{L} \right) \left( \frac{T}{T_0} \right)^{km} \left[ \frac{2\alpha T}{km} \right]^2 (1 + \lambda V_{GS,P3}) \]

When \( km \) equals to -2

\[ I_{D,P3} = \frac{1}{2} \mu_0 C_{OX} \left( \frac{W}{L} \right) (\alpha T_0)^2 (1 + \lambda V_{GS,P3}) \]

Through the help of the current mirrors (P1, P2) and (N1, N2), NOT conduction current kept thermally insensitive, too
The thermal sensitivity of TRDL is not required to be exactly zero which is very hard to achieve. Only propagation delay difference between the two delay lines large enough is required. This greatly reduces the design difficulty and enhances the tolerance to process variation.
Modified Temperature-to-Pulse Generator

- Less offset

\[ T_p \]

\[ \text{START} \]

- Temperature Dependent Delay Line
- Temperature Reference Delay Line

XOR

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Cyclic TDC

- **Pulse-shrinking delay cell used**
  - Shrinking controlled by the aspect ratios of adjacent cells
Experimental Results

- TDDL delay > TRDL delay
- LSB = 0.16°C, INL = -0.7~0.9°C
- 0.175mm², 10μW @ 2 samples/s

[P. Chen, JSSC 2005]
measurement results of 25 test chips

Error after 2-point calibration
Smart Temperature Sensor with Negative Temperature Coefficient

- **TDDL delay < TRDL delay**
  - Linearity: TRDL better than TDDL
  - Every compensation circuit shared by two NOT gates → compensation circuits halved
    - Both chip size & power consumption reduced
Experiment Results

[C.-C. Chen, MST 2006]
What Next

- Full Digitization
- Better Accuracy
- Less Power Consumption
- Smaller die size
- Cheaper calibration cost for mass production
- More applications
Time-Domain SAR Smart temperature sensor

- The most accurate time-domain one till now
- Size: 0.6 mm\(^2\) in a 0.35\(\mu\)m
- Current: 11.12 \(\mu\)A
- Error:-0.25\(^\circ\)C\,-0.35\(^\circ\)C for 26 chips
Closer Look

Digital Thermostat

Start

Offset Time Cancellation Circuit

Temperature Dependent Delay Line

Adjustable Reference Delay Line

Time Comparator

Set-Point

SAR Control Logic

Digital Output

Delay Time

Trip Temperature

Delay Time

Trip Temperature

TA

TD

T_D

T_A

T_ref

D9 : D0

CLK

Closer Look
Exemplified Operation of the 4-bit Time-Domain SAR Sensor

Game Over

Step 0 (1000)
Step 1 (1100)
Step 2 (1110)
Step 3 (1011)
Step 4 (1100)

$T_{MAX} + T_{BASE}$

$3/4T_{MAX} + T_{BASE}$

$1/2T_{MAX} + T_{BASE}$

$1/4T_{MAX} + T_{BASE}$

$T_{BASE}$

Conversion Steps

Delay

Conversion Steps

$T_D$
Temperature Dependent Delay Line
Adjustable Reference Delay Line
SAR Control Logic
Time Offset Cancellation Circuit
Time Comparator

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[P. Chen, JSSC 2010]
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Analog vs. Digital

Analog signal

Digitized signal

$V(t)$

Time
## Analogue versus Digital

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<tr>
<th></th>
<th>Analog Design</th>
<th>Digital Design</th>
</tr>
</thead>
<tbody>
<tr>
<td>Signal</td>
<td>Continuous</td>
<td>Discrete</td>
</tr>
<tr>
<td>Design</td>
<td>Customized</td>
<td>Standardized</td>
</tr>
<tr>
<td>Model requirement</td>
<td>Precise model</td>
<td>Abstract model</td>
</tr>
<tr>
<td>Programmability</td>
<td>Hard to change</td>
<td>Programmable by software</td>
</tr>
<tr>
<td>Design level</td>
<td>Circuit level</td>
<td>System level</td>
</tr>
<tr>
<td>CAD tools</td>
<td>Difficult to use with CAD tools</td>
<td>Amenable to CAD tools</td>
</tr>
<tr>
<td>Complexity</td>
<td>Too many design parameters</td>
<td>Simple and easy</td>
</tr>
</tbody>
</table>
Going from Analogue to Digital

- Few analog applications can be fully digitized
  - TDC
  - PLL
  - DLL
  - Frequency synthesizer
  - …

- Even fewer can be realized in FPGA with performance comparable to analog ones
  - No bias or device sizing allowed

- Convention always means no innovation
  - Think big, do small
Digitization and FPGA Realization

**Why Digital**
- Compatible to cell-based design
- Easy to port among processes

**Why FPGA**
- More and more built-in analogue blocks
- Fast prototyping

![Comparison of Conventional vs Current Distribution](image_url)
FPGA Smart Temperature Sensor

- First FPGA thermal sensor
- Pure cell-based design
- Only 140 LEs used
- INL Error: -1.5~0.8°C for 0~75°C range
- Power: 8.4µW
Effective measurement errors of 10 FPGA chips with two-temperature calibration

[P. Chen, TCAS-I 2007]
Improved FPGA smart sensor

- Replace cyclic delay line with retriggerable ring oscillator
- No fixed pulse generator required, better accuracy
- Time amplifier gain: from fixed to variable
  - 1-point calibration support
- Only 48 LEs used

[Start]

Output Counter

CLK

Digital Output (D_{out})

On-Chip

SAR Control Logic

Comparator

A>B

N

m

D_{out,0}

Reset

Comp

Retriggerable Ring Oscillator

Enable

Time Amplifier

D_{out,0}

Digital Output (D_{out})

[65]

P. Chen, TCAS-I 2011

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Retriggerable ring oscillator

Variable-gain time amplifier
One-Point Calibration

- Off-chip calibration circuit for cost down
- All chips calibrated to have same output at a calibration temperature
- 2nd-order master curve used for temperature interpretation
Measured Results

- 20 test chips spreading over 4 years
- Error: -0.7~0.6°C
- Conversion rate: 4.4k
- Min. power: 175nW

FPGA test board with retail price < US$ 100

Measured inaccuracy according to the 2nd-order master curve
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Key Requirements to Success

- IQ is not everything
  - NTU ➔ NTHU ➔ ............ NTUST
  - MIT ➔ ................................ NTU......................... NTUST

- Insufficient resource is not a good excuse
  - What’s left for little monks in little temples

- EQ is much more important
  - Innovation
    - Think big and different
  - Hard-working, hard-working and hard-working ...
Something Important to Remind

http://www.wretch.cc/blog/markleeblog
Finally …

Trust me, you can make it!
Even impossible says I’m possible.
Thanks for Your Attention